REMARKS

Rejection of Claim 1 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

In response to the rejection made on Claim 1 under U.S.C 102b as being anticipated by Zhou et al. (US 5,913,924) the applicant has provided the following response:

Although Zhou et al. does teach a microcontroller with expandable memory banks, applicant asserts that Zhou et al. do not teach each and every element of the present invention because Zhou et al. utilize a different architecture having correspondingly different functionality than that described and claimed in the present invention. For at least this reason, applicant asserts that the present invention as claimed in claim 1 should not be found anticipated by Zhou et al. Further remarks illustrating specific differences between the present invention and the teachings of Zhou et al. are detailed below.

Of particular note, applicant stresses that Zhou et al. do not teach a memory bank control circuit connected to the microprocessor for asserting a signal during the processing of an interrupt, as recited in the limitation of claim 1. The Examiner has suggested in the office action that the space selection signal (instruction) asserted by the interrupt service routine (Col 6 lines 49-64) is comparable. Zhou et al. also teach, "if an interrupt occurs…a space selection instruction is used to switch to the first code bank and service the interrupt" (Col6 lines 50-55), however Zhou et al. further add "Specifically, microprocessor 310…jumps to interrupt passing instructions 570" (Col 7 lines 25-27) and "Interrupt passing instructions 570 include a space selection instruction … that switches execution to code bank 370A" (Col 7 lines 28-30). Therefore applicant asserts through deduction, that it is in fact the microprocessor 310 (emphasis added) of Zhou et al. that asserts the space selection signal during an interrupt. This is in contrast to the present invention, which provides a memory

bank control circuit for asserting a signal during the processing of an interrupt. Furthermore, Zhou et al. teach using a microprocessor for asserting the space selection signal through a software process, whereas the present invention provides a hardware based memory bank control circuit (independent of the microprocessor) to assert the signal during an interrupt.

Regarding the multiplexer of claim 1, applicant asserts that Zhou et al. do not provide a multiplexer for connecting the microprocessor to the plurality of memory banks. Inspection of Figs. 2 and 3 from the disclosure of Zhou et al. will verify that no such component is provided. According to the present invention, the multiplexer plays an important role in switching between memory banks. The multiplexer selects between the page selection signal for use during normal operation, and a predetermined bank value corresponding to the interrupt service routine (ISR) during an interrupt. One of these signals is then sent to the plurality of memory banks to allow for a particular memory bank to be accessed by the microcontroller according to the selected signal. Therefore, during an interrupt, the multiplexer and memory bank control circuit work in conjunction to immediately switch memory banks through hardware.

The claimed architecture of the present invention contrasts that taught by Zhou et al., and because Zhou et al. do not include the same hardware elements as the present invention claimed in claim 1, they are unable to immediately switch memory banks because they teach using a software method to switch memory banks. According to Zhou et al., if the currently accessed memory bank does not contain the ISR, it "is encoded with interrupt passing instructions 570 that include a space selection instruction to switch to the first code bank 370A" (Col 7, lines15-17), and "on occurrence of the interrupt...microprocessor 310 switches to the first code bank" (Col 7, lines 19-22). Therefore, following the same rationale as described above, the microprocessor must assert the space selection instruction to change memory banks as a software process upon the occurrence of an interrupt. Furthermore, because a software process involves the reading and execution of code (being the space

selection instruction), a certain amount of time must be expended prior to a memory bank switch. Thus the switching of memory banks does not occur immediately through the teachings of Zhou et al.. This is in contrast to the present invention as claimed in claim 1, where the hardware apparatus (multiplexer and memory bank control circuit) is specifically used to allow for an immediate switch of memory banks upon an interrupt. Also, by virtue of utilizing the multiplexer and memory bank control circuit, the present invention as claimed in claim 1 does not require a space selection instruction in each memory bank to switch memory banks upon an interrupt. This reduces overall memory consumption in the memory banks, allowing for more memory to be used for data storage and microcontroller processes.

In summary, the present invention as claimed in claim includes a memory bank control circuit and a multiplexer to automatically and immediately switch, through hardware, a currently accessed memory bank to the memory bank containing the ISR upon an interrupt. This is in contrast to the teachings of Zhou et al., who do not provide a memory bank control circuit and multiplexer. Zhou et al. teach a method of implementing space selection instructions in each memory bank, and upon an interrupt, executing the space selection instruction though a software process of the microcontroller to switch memory banks. Use of the memory bank control circuit and multiplexer in the present invention allow the switching of memory banks during an interrupt to be performed independently of the microprocessor, helping alleviate microcontroller (software) resources otherwise required for switching memory banks.

For at least the above-mentioned reasons, applicant asserts that the present invention and the teachings of Zhou et al. differ greatly in structure and methodology. Applicant kindly requests that the Examiner re-evaluate claim 1 in light of the above remarks in order to make for its allowance.

Rejection of Claims 2-3 under U.S.C. 102(b) as being anticipated by Zhou et al (US

5,913,924)

Regarding claims 2-3, applicant asserts that these claims are dependant upon claim 1. Therefore, should an allowance be made for claim 1, applicant kindly requests that allowances also be made for claims 2 and 3 as they are dependant upon claim 1.

Rejection of Claim 4 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

In regards to claim 4, applicant asserts that Zhou et al. do not teach a multiplexer (see remarks for claim 1). Therefore, Zhou et al. cannot teach providing an extra input for a different predetermined page selection signal to the multiplexer. Furthermore, the Examiner has suggested that the space select signal of Zhou et al. is comparable to the different predetermined page selection signal corresponding to the memory bank storing different interrupt service routines (ISR), according to the limitation of claim 4. However Zhou et al. state "a space selection instruction is used to switch to the first code bank and service the interrupt" (Col 6 lines52-55) and "Although handling of only one interrupt has been discussed... other interrupts can also be handled similarly if the corresponding interrupt services routines are encoded in code bank 370A " (Col 7 lines 64-70), wherein only bank 370A contains the interrupt service routine (Col 6 line 57). Therefore according to Zhou et al., an additional interrupt service routine must be placed in the same memory bank (Bank 370A) in order for an additional interrupt service to function. This is in contrast to the present invention, where the different interrupt service routine can be placed into any memory bank, and the different predetermined page selection signal references the location of the different interrupt service routine regardless of which memory bank it is located. In summary, the space selection signal of Zhou et al. corresponds only to the memory bank storing the ISR, and not necessarily that of the different ISR. This is in contrast to the present invention, wherein the different

predetermined page selection signal does correspond to the memory bank storing the different ISR, as disclosed in the limitation for claim 4.

For at least the above-mentioned reasons, applicant kindly requests that the Examiner re-evaluate claim 4 in light of the above remarks in order to make for its allowance.

Rejection of Claim 5 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

Applicant asserts that Zhou et al. do not teach a memory bank control circuit (see remarks for claim 1) as claimed in the present invention. Additionally, applicant asserts that the selection signal of the present invention uniquely corresponds to a specific interrupt source, as is recited in claim 5. The Examiner has suggested in remarks for claim 5 that the space select instruction of Zhou et al. also similarly corresponds to a different interrupt sources. However, taking into consideration remarks made for Claim 4, applicant asserts that the selection signal of Zhou et al. is not unique, and only corresponds to the memory bank storing the main ISR (for bank switching) regardless of which interrupt may have occurred. Zhou et al. teach "a space selection instruction is used to switch to the first code bank and service the interrupt" (Col 6 lines52-55) and "Although handling of only one interrupt has been discussed... other interrupts can also be handled similarly if the corresponding interrupt services routines are encoded in code bank 370A " (Col 7 lines64-70), wherein only bank 370A contains the main interrupt service routine (Col 6 line 57). This is in contrast to the present invention, whereas the selection signal can be unique, and can correspond to a unique memory bank according a unique interrupt source.

In summary, the space select instruction of Zhou et al. is not unique, and when executed will result in bank switching to the bank storing the main ISR regardless of which interrupt has occurred and where the desired ISR is located. Therefore, the space select instruction does not provide a unique response according to one of different interrupt sources. This is in contrast to the present invention, which provides a unique selection signal directly corresponding to a specific interrupt that has occurred. The uniqueness of the selection signal is highlighted by the fact that it can represent a specific

memory bank according to the particular interrupt (see remarks for claim 4), whereas the selection signal of Zhou et al. is not unique and solely corresponds to the memory bank storing the main ISR regardless of which particular interrupt has occurred.

Rejection of Claim 6-7 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

Regarding claims 6-7, applicant asserts that these claims are dependant upon claim 1. Therefore, should an allowance be made for claim 1, applicant kindly requests that allowances also be made for claims 6 and 7 as they are dependant upon claim 1.

Rejection of Claim 8 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

Claim 8 has been amended by the applicant in order to more distinctly describe the method of the present invention. No new subject matter was added or introduced as a result of this amendment. Step (a) has been amended to clearly illustrate that an interrupt service routine (ISR) is only stored into one memory bank of the plurality of memory banks. Step (b) has been amended to highlight the fact that selection and access of a memory bank containing the ISR occurs immediately after an interrupt, and that the predetermined page selection signal is output from the microprocessor.

Applicant asserts that during an interrupt (step (c)), Zhou et al. does not teach immediately selecting and accessing the memory bank containing the ISR. Zhou et al. teach "if an interrupt occurs in a code bank other than the first code bank, a space selection instruction is used to switch to the first code bank and service the interrupt" (Col 6 lines 52-55). Therefore, execution of the space selection instruction is an intermediate step that must be performed prior to bank switching. Execution of the space selection instruction further requires use of microcontroller resources (Col 6 lines 33-40) to read and execute the instruction. This inherently results in a finite delay before actual bank switching can occur, rendering the switching of banks non-immediate.

Furthermore, applicant asserts that Zhou et al. do not teach a predetermined page selection signal output by the microprocessor to switch memory banks, as recited in the limitation for newly amended claim 8. Zhou et al. teach referencing "a space selection instruction...to switch to the first code bank and service the interrupt" (Col 6 lines 52-55). However, the space selection instruction is obtained from the select-instruction storage element (Fig 3 elements 375A/B, Col 5 line 26), and not outputted by the microprocessor. Therefore, the invention of Zhou et al. do not access a memory bank according to a

predetermined page selection signal output by the microprocessor.

In summary, the method of Zhou et al. does not immediately select and access the memory bank storing the interrupt service routines because it must execute a space selection instruction as an intermediate step. Also, the accessing and selecting of memory banks does not reference a predetermined page selection signal output by the microprocessor, as it references the space selection instruction in the select-instruction storage element.

For at least the above-mentioned reasons, applicant asserts that the present invention as claimed in currently amended claim 8 should not be found anticipated by the teachings of Zhou et al. Applicant kindly requests that the Examiner evaluate currently amended claim 8 in light of the above remarks in order to make for its allowance.

Rejection of Claim 9-11 under U.S.C. 102(b) as being anticipated by Zhou et al (US 5,913,924)

Regarding claims 9-11, applicant asserts that these claims are dependant upon claim 8. Therefore, should an allowance be made for claim 8, applicant kindly requests that allowances also be made for claims 9-11 as they are dependant upon claim 8.

Introduction of new claims 12-22

Applicant has introduced new claims 12-22 to more distinctly define and describe the apparatus and device of the present invention. Introduction of these claims is fully supported in the current specification as illustrated in Figures 2-3 with no new material or additional subject matter included. Applicant would like to particularly highlight the

differences between the following new independent claims and the teachings of Zhou et al.

Claim 12 includes a microcontroller with expandable memory banks. The microprocessor in this claim continually outputs a page selection signal to access a particular memory bank under normal operation, and a predetermined value corresponding to the memory bank storing the interrupt service routine. When an interrupt occurs, the microprocessor will additionally assert an interrupt signal. The multiplexer receives the page selection signal and the predetermined value, and outputs one of these as a selection signal. The memory bank control circuit toggles the selection of the multiplexer inputs, and selects the predetermined value as the selection signal when the interrupt signal is asserted, and selects the page selection signal as the selection signal when the interrupt signal is not asserted. The plurality of memory banks allows the microprocessor to access a particular memory bank according to the selection signal.

In this way, the multiplexer and memory bank control circuit completely and immediately handle the switching of the memory banks when the interrupt service routine when an interrupt occurs. This allows the microprocessor to immediately access the desired interrupt service routine without any software delay. Additionally, microprocessor resources are alleviated using this configuration. Because bank switching is conducted completely in hardware, the microprocessor is allowed to focus on other additional processes. Furthermore, space selection instructions are not required to be stored into every memory bank as required for software-based bank switching methods. This reduces memory consumption, and allows increases overall useable memory by the microprocessor.

This is in contrast to the teachings of Zhou et al, as they do not teach utilizing hardware components (being the multiplexer and memory bank control circuit in the

present invention) to execute the switching of memory banks. Because Zhou et al. rely on a software switching routine involving the execution of a space selection instruction, switching cannot occur immediately as the instruction must be first be loaded then executed by the microprocessor. Furthermore, Zhou et al. teaches the storing of a space selection instruction in every memory bank in order to switch memory banks. This results in a reduced availability of overall memory, as a portion of memory must be allocated for the space selection instruction in every memory bank. Because the present invention performs this task in hardware, such an instruction code is not required, allowing otherwise allocated memory to be utilized for data and other processes.

Claim 19 is a method claim analogous to device claim 12. This claimed method comprises asserting a page selection signal, and a predetermined value corresponding to a memory bank storing an interrupt service routine (ISR). One of these two signals is then selected to be the selection signal, the choice depending on the occurrence of an interrupt signal. A particular memory bank can be then accessed by the microcontroller, the memory bank corresponding to the chosen selection signal.

Because the page selection signal and predetermined value are continually outputted, this allows for an immediate switch of memory banks upon the occurrence of an interrupt signal. Additionally, this method does not require the use of variables or instructions to be stored into memory banks, as key parameters and signals are outputted directly from the microprocessor. Furthermore, this method allows the memory bank locations to be easily updated by the microprocessor should an additional interrupt be utilized or changed.

This is in contrast to the teachings of Zhou et al. as they do not teach the continual assertion of a page selection signal, and a predetermined value corresponding to the memory bank with the ISR. Zhou et al. teach storing the desired memory bank into current space storage element 251 for normal operation, and upon an interrupt, switching

to a main memory bank according to the space selection instruction. Because a desired memory bank value must be stored into current space storage element 251, this would require at least an instruction step of the microprocessor before memory banks are switched resulting in a finite delay before switching. Furthermore, utilization of the space selection instruction for switching banks upon an interrupt makes it difficult to change the memory bank where the ISR is located. This is because the space selection instruction would have to be reprogrammed beforehand in order to change the location of the ISR.

Because claims 13-18 and 20-22 are dependent on the above described new independent claims 12 and 19, respectively, if claims 12 and 19 are found allowable, so too should the corresponding dependent claims. Consideration of new claims 12-22 is respectfully requested.

Sincerely yours,

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